WHAT IS CLAIMED IS:

1. A variable gain differential amplifier comprising:

a variable impedance circuit;

a first transistor having a first terminal receiving a first input signal, a second terminal connected to a first potential through a first load and a third terminal connected to said variable impedance circuit; and

a second transistor having a first terminal receiving a second input signal, a second terminal connected to said first potential through a second load and a third terminal connected to said variable impedance circuit,

said variable impedance circuit including:

one or more first resistive elements connected between said third terminal of said first transistor and a second potential,

one or more second resistive elements connected between said third terminal of said second transistor and said second potential, and

a plurality of variable impedance devices connected between one end of at least one said first resistive element and one end of at least one said second resistive element and between the other end of said at least one first resistive element and the other end of said at least one second resistive element respectively and having control terminals receiving

a common control voltage.

2. The variable gain differential amplifier according to claim 1, wherein

said one or more first resistive elements include:

a first resistor connected between said third terminal of said first transistor and a first node, and

a second resistor connected between said first node and a second node receiving said second potential,

said one or more second resistive elements include:

a third resistor connected between said third terminal of said second transistor and a third node, and

a fourth resistor connected between said third node and a fourth node receiving said second potential, and

said plurality of variable impedance devices include:

a first variable impedance device connected between said third terminal of said first transistor and said third terminal of said second transistor, and

a second variable impedance device connected between said first node and said third node.

3. The variable gain differential amplifier according to claim 1, wherein

said one or more first resistive elements include a first resistor connected between said third terminal of said first

transistor and a first node receiving said second potential,

said one or more second resistive elements include a second resistor connected between said third terminal of said second transistor and a second node receiving said second potential, and

said plurality of variable impedance devices include:

a first variable impedance device connected between said third terminal of said first transistor and said third terminal of said second transistor, and

a second variable impedance device connected between said first node and said second node.

4. The variable gain differential amplifier according to claim 1, wherein

said one or more first resistive elements include:

a first resistor connected between said third terminal of said first transistor and a first node,

a second resistor connected between said first node and a second node, and

a third resistor connected between said second node and a third node receiving said second potential,

said one or more second resistive elements include:

a fourth resistor connected between said third terminal of said second transistor and a fourth node,

a fifth resistor connected between said fourth node and

a fifth node, and

a sixth resistor connected between said fifth node and a sixth node receiving said second potential, and

said plurality of variable impedance devices include:

a first variable impedance device connected between said first node and said fourth node, and

a second variable impedance device connected between said second node and said fifth node.

5. The variable gain differential amplifier according to claim 1, wherein

said one or more first resistive elements include:

a first resistor connected between said third terminal of said first transistor and a first node, and

a second resistor connected between said first node and a second node receiving said second potential,

said one or more second resistive elements include:

a third resistor connected between said third terminal of said second transistor and a third node, and

a fourth resistor connected between said third node and a fourth node receiving said second potential, and

said plurality of variable impedance devices include:

a first variable impedance device connected between said first node and said third node, and

a second variable impedance device connected between

said second node and said fourth node.

6. A multiplication circuit comprising:

first, second, third, fourth, fifth and sixth transistors each having a first terminal, a second terminal and a third terminal; and

a variable impedance circuit, wherein

said first terminal of said first transistor receives a first input signal, said second terminal of said first transistor is connected to a first potential through a first load and said third terminal of said first transistor is connected to said second terminal of said fifth transistor,

said first terminal of said second transistor receives a second input signal, said second terminal of said second transistor is connected to said first potential through a second load and said third terminal of said second transistor is connected to said second terminal of said fifth transistor,

said first terminal of said third transistor receives said second input signal, said second terminal of said third transistor is connected to said first potential through said first load and said third terminal of said third transistor is connected to said second terminal of said sixth transistor,

said first terminal of said fourth transistor receives said first input signal, said second terminal of said fourth transistor is connected to said second potential through said

second load and said third terminal of said fourth transistor is connected to said second terminal of said sixth transistor,

said first terminal of said fifth transistor receives a third input signal,

said first terminal of said sixth transistor receives a fourth input signal, and

said variable impedance circuit includes:

one or more first resistive elements connected to said third terminal of said fifth transistor and said second potential,

one or more second resistive elements connected to said third terminal of said sixth transistor and said second potential, and

a plurality of variable impedance devices connected between one end of at least one said first resistive element and one end of at least one said second resistive element and between the other end of said at least one first resistive element and the other end of said at least one second resistive element respectively and having control terminals receiving a common control voltage.

7. The multiplication circuit according to claim 6, wherein

said one or more first resistive elements include:

a first resistor connected between said third terminal

of said fifth transistor and a first node, and

a second resistor connected between said first node and a second node receiving said second potential,

said one or more second resistive elements include:

a third resistor connected between said third terminal of said sixth transistor and a third node, and

a fourth resistor connected between said third node and a fourth node receiving said second potential, and

said plurality of variable impedance devices include:

a first variable impedance device connected between said third terminal of said fifth transistor and said third terminal of said sixth transistor, and

a second variable impedance device connected between said first node and said third node.

8. The multiplication circuit according to claim 6, wherein

said one or more first resistive elements include a first resistor connected between said third terminal of said fifth transistor and a first node receiving said second potential,

said one or more second resistive elements include a second resistor connected between said third terminal of said sixth transistor and a second node receiving said second potential, and

said plurality of variable impedance devices include:

a first variable impedance device connected between said third terminal of said fifth transistor and said third terminal of said sixth transistor, and

a second variable impedance device connected between said first node and said second node.

9. The multiplication circuit according to claim 6, wherein

said one or more first resistive elements include:

a first resistor connected between said third terminal of said fifth transistor and a first node,

a second resistor connected between said first node and a second node, and

a third resistor connected between said second node and a third node receiving said second potential,

said one or more second resistive elements include:

a fourth resistor connected between said third terminal of said sixth transistor and a fourth node,

a fifth resistor connected between said fourth node and a fifth node, and

a sixth resistor connected between said fifth node and a sixth node receiving said second potential, and

said plurality of variable impedance devices include:

a first variable impedance device connected between said first node and said fourth node, and

a second variable impedance device connected between said second node and said fifth node.

10. The multiplication circuit according to claim 6, wherein

said one or more first resistive elements include:

a first resistor connected between said third terminal of said fifth transistor and a first node, and

a second resistor connected between said first node and a second node receiving said second potential,

said one or more second resistive elements include:

a third resistor connected between said third terminal of said sixth transistor and a third node, and

a fourth resistor connected between said third node and a fourth node receiving said second potential, and

said plurality of variable impedance devices include:

a first variable impedance device connected between said first node and said third node, and

a second variable impedance device connected between said second node and said fourth node.

11. A variable gain differential amplifier comprising:

a first transistor having a first terminal receiving a first input signal, a second terminal connected to a first potential through a first load and a third terminal connected

to a second potential through a second load;

a second transistor having a first terminal receiving a second input signal, a second terminal connected to said first potential through a third load and a third terminal connected to said second potential through a fourth load; and

a variable impedance circuit connected between said third terminal of said first transistor and said third terminal of said second transistor,

said variable impedance circuit including:

a plurality of first variable impedance devices serially connected between said third terminal of said first transistor and said third terminal of said second transistor, and

at least one second variable impedance device that is connected between a node between said plurality of first variable impedance devices and said second potential and is turned on/off complementarily to said plurality of first variable impedance devices.

12. The variable gain differential amplifier according to claim 11, further comprising an output terminal connected to said second terminal of said second transistor for deriving an output signal.

13. The variable gain differential amplifier according to claim 11, further comprising:

a first output terminal connected to said second terminal of said first transistor for deriving a first output signal, and

a second output terminal connected to said second terminal of said second transistor for deriving a second output signal.

14. The variable gain differential amplifier according to claim 11, further comprising:

an input terminal receiving said first input signal for supplying said first input signal to said first terminal of said first transistor, and

an inversion circuit that inverts said first input signal from said input terminal for supplying the inverted first input signal to said first terminal of said second transistor as said second input signal.

15. A multiplication circuit comprising:

first, second, third, fourth, fifth and sixth transistors each having a first terminal, a second terminal and a third terminal; and

a variable impedance circuit, wherein

said first terminal of said first transistor receives a first input signal, said second terminal of said first transistor is connected to a first potential through a first

load and said third terminal of said first transistor is connected to said second terminal of said fifth transistor,

said first terminal of said second transistor receives a second input signal, said second terminal of said second transistor is connected to said first potential through a second load and said third terminal of said second transistor is connected to said second terminal of said fifth transistor,

said first terminal of said third transistor receives said second input signal, said second terminal of said third transistor is connected to said first potential through said first load and said third terminal of said third transistor is connected to said second terminal of said sixth transistor,

said first terminal of said fourth transistor receives said first input signal, said second terminal of said fourth transistor is connected to said first potential through said second load and said third terminal of said fourth transistor is connected to said second terminal of said sixth transistor,

said first terminal of said fifth transistor receives a third input signal and said third terminal of said fifth transistor is connected to a second potential through a third load,

said first terminal of said sixth transistor receives a fourth input signal and said third terminal of said sixth transistor is connected to said second potential through a fourth load, and

said variable impedance circuit includes:

a plurality of first variable impedance devices serially connected between said third terminal of said fifth transistor and said third terminal of said sixth transistor, and

at least one second variable impedance device that is connected between a node between said plurality of first variable impedance devices and said second potential and is turned on/off complementarily to said plurality of first variable impedance devices.

16. The multiplication circuit according to claim 15, further comprising an output terminal connected said second terminals of said second and fourth transistors for deriving an output signal.

17. The multiplication circuit according to claim 15, further comprising:

a first output terminal connected to said second terminals of said first and third transistors for deriving a first output signal, and

a second output terminal connected to said second terminals of said second and fourth transistors for deriving a second output signal.

18. The multiplication circuit according to claim 15,

further comprising:

a first input terminal receiving said first input signal for supplying said first input signal to said first terminals of said first and fourth transistors,

a first inversion circuit that inverts said first input signal from said first input terminal for supplying the inverted first input signal to said first terminals of said second and third transistors as said second input signal,

a second input terminal receiving said third input signal for supplying said third input signal to said first terminal of said fifth transistor, and

a second inversion circuit that inverts said third input signal from said second input terminal for supplying the inverted third input signal to said first terminal of said sixth transistor as said fourth input signal.